NCE40P70K

P-Channel Enhancement Mode Power MOSFET

Description

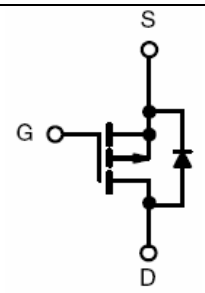
The NCE40P70K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge .This device is well suited for high current load applications.

General Features

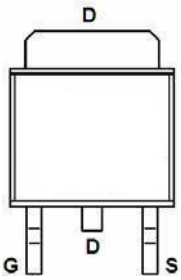
- V_{DS} =-40V,I_D =-70A
  $R_{DS(ON)}$ <10mΩ @ V_{GS}=-10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

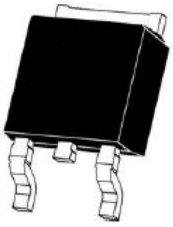
- Power switch
- Load switch in high current applications
- DC/DC converters



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE40P70K	NCE40P70K	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-70	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-49.5	A
Pulsed Drain Current	I_{DM}	-200	A
Maximum Power Dissipation	P_D	130	W
Derating factor		1.04	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	1012	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	0.96	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

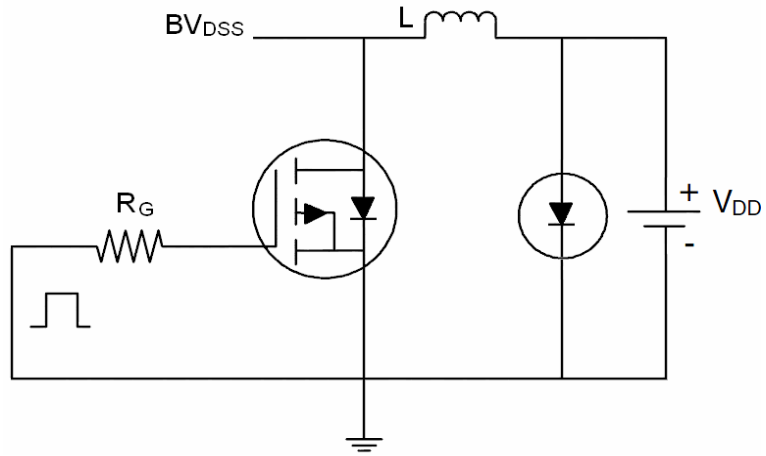
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.2	-1.9	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-20A	-	7.5	10	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-10V,I_D=-20A	-	50	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-20V,V_{GS}=0V, F=1.0MHz	-	5380	-	PF
Output Capacitance	C_{oss}		-	570	-	PF
Reverse Transfer Capacitance	C_{rss}		-	500	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-20V, R_L=2Ω, V_{GS}=-10V,R_G=1Ω	-	15	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	70	-	nS
Turn-Off Fall Time	t_f		-	18	-	nS
Total Gate Charge	Q_g	V_{DS}=-20,I_D=-20A, V_{GS}=-10V	-	106		nC
Gate-Source Charge	Q_{gs}		-	22		nC
Gate-Drain Charge	Q_{gd}		-	27		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-70A	-		-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-70	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =- 70A di/dt = -100A/μs(Note3)	-	53		nS
Reverse Recovery Charge	Qrr		-	50		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

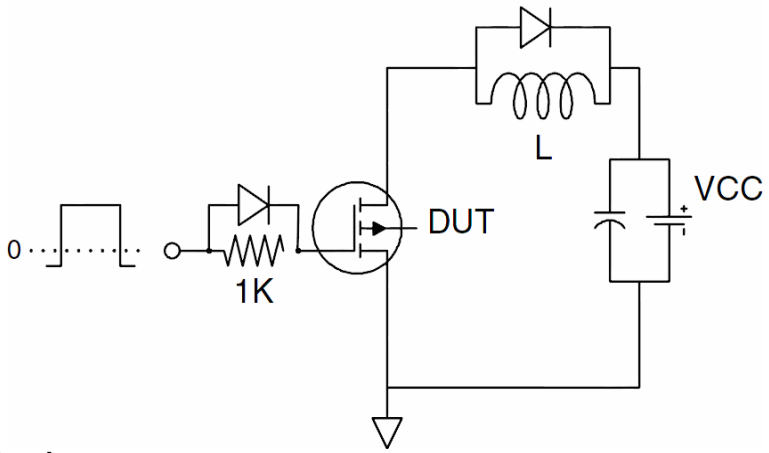
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: Tj=25℃,V_{DD}=-20V,V_G=-10V,L=1mH,Rg=25Ω,I_{AS}=45A

Test Circuit

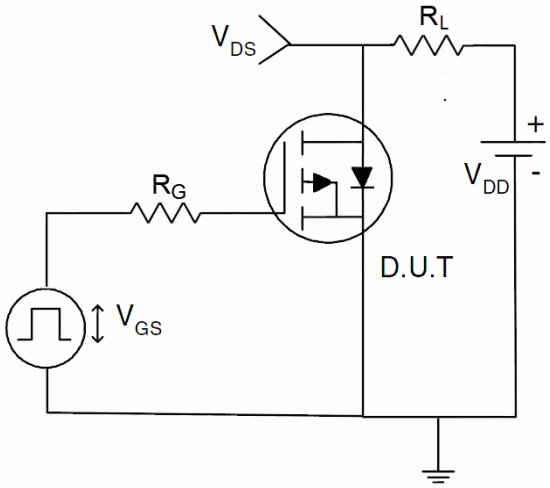
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

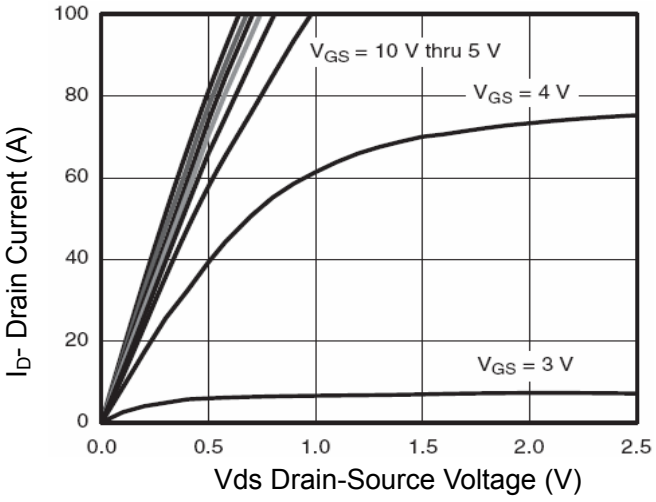


Figure 1 Output Characteristics

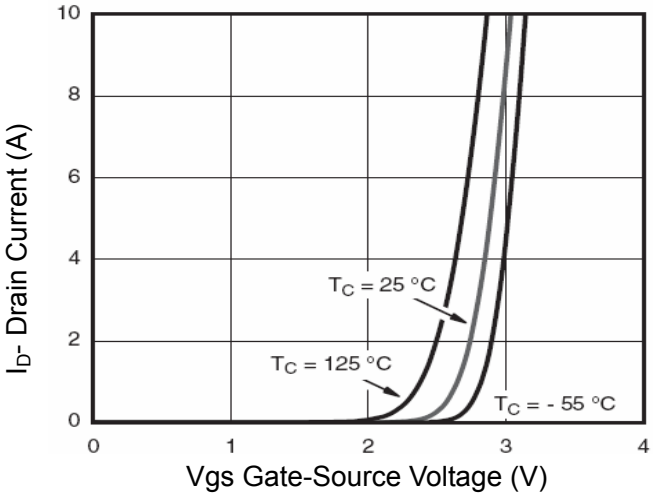


Figure 2 Transfer Characteristics

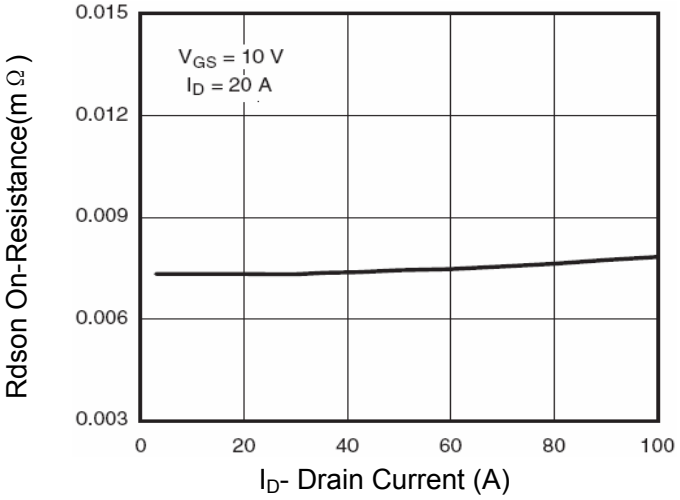


Figure 3 Rdson- Drain Current

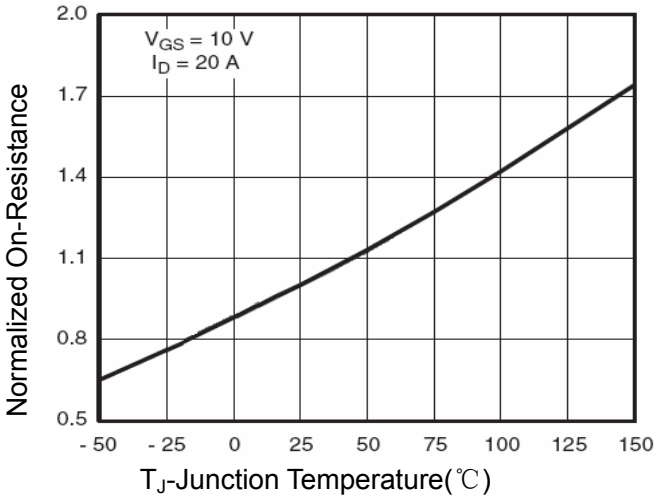


Figure 4 Rdson-Junction Temperature

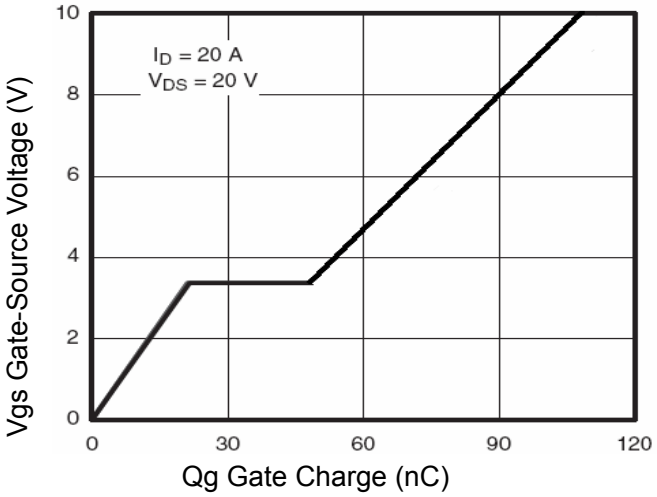


Figure 5 Gate Charge

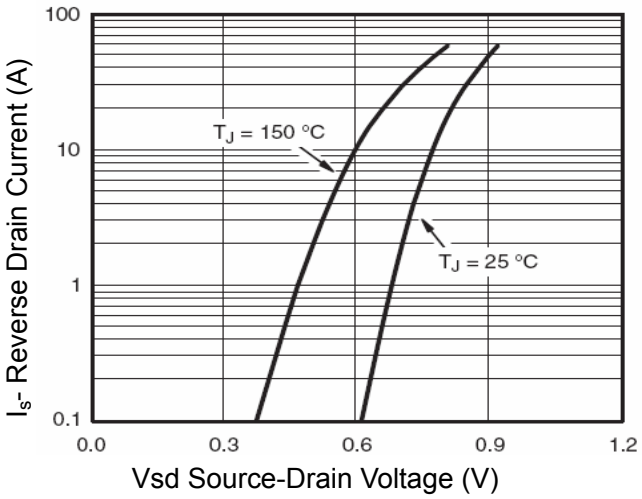


Figure 6 Source- Drain Diode Forward

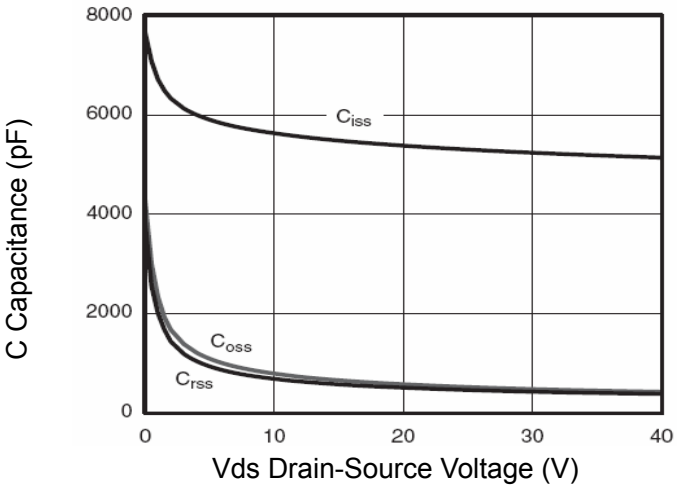


Figure 7 Capacitance vs Vds

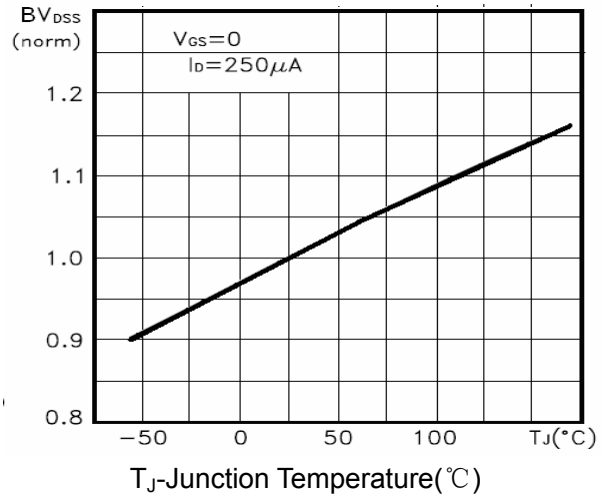


Figure 9 BV_{DSS} vs Junction Temperature

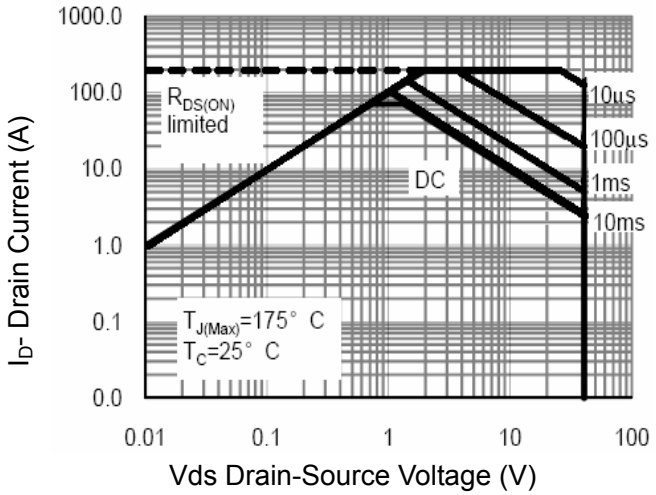


Figure 8 Safe Operation Area

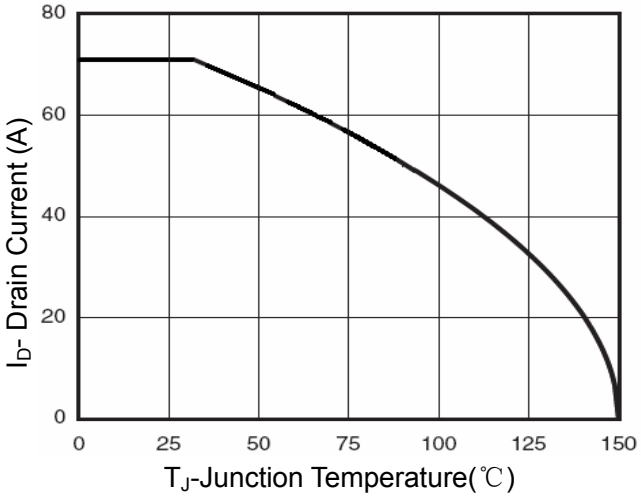


Figure 10 ID Current Derating vs Junction Temperature

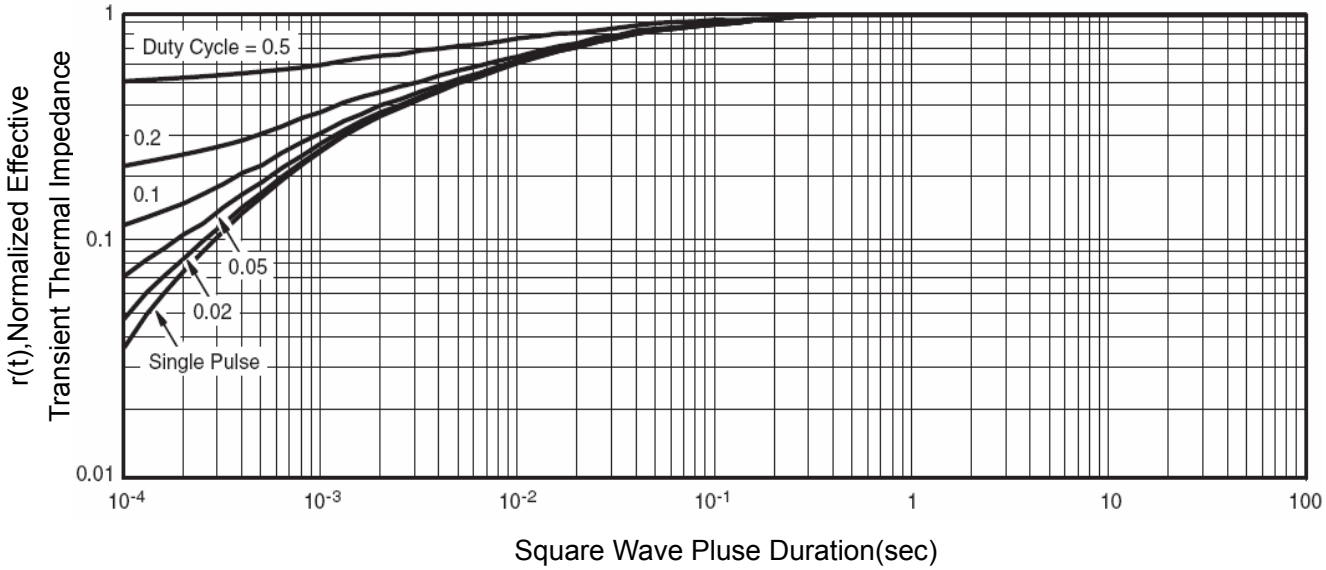


Figure 11 Normalized Maximum Transient Thermal Impedance