

Low Capacitance Diode Array for ESD Protection in Four Data Lines

SZ/NUP4301MR6T1G is a micro-integrated device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).

Features

- Low Capacitance (1.5 pf Maximum Between I/O Lines)
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
Machine Model = Class C
Human Body Model = Class 3B
- Protection for IEC61000-4-2 (Level 4)
8.0 kV (Contact)
15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device*

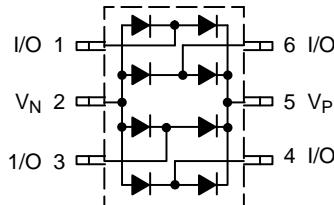
Applications

- USB 1.1 and 2.0 Data Line Protection
- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I²C Bus Protection

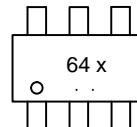


SC-74
CASE 318F

PIN CONFIGURATION AND SCHEMATIC



MARKING DIAGRAM



MAXIMUM RATINGS (Each Diode) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	70	Vdc
Forward Current	I_F	200	mAdc
Peak Forward Surge Current	$I_{FM(\text{surge})}$	500	mAdc
Repetitive Peak Reverse Voltage	V_{RRM}	70	V
Average Rectified Forward Current (Note 1) (averaged over any 20 ms period)	$I_{F(\text{AV})}$	715	mA
Repetitive Peak Forward Current	I_{FRM}	450	mA
Non-Repetitive Peak Forward Current $t = 1.0 \mu\text{s}$ $t = 1.0 \text{ ms}$ $t = 1.0 \text{ S}$	I_{FSM}	2.0 1.0 0.5	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-5 = 1.0 × 0.75 × 0.062 in.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	°C/W
Lead Solder Temperature, Maximum 10 Seconds Duration	T_L	260	°C
Junction Temperature	T_J	-40 to +150	°C
Storage Temperature	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (Each Diode)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Reverse Breakdown Voltage ($I_{(BR)} = 100 \mu\text{A}$)	$V_{(BR)}$	70	-	-	Vdc
Reverse Voltage Leakage Current ($V_R = 70 \text{ Vdc}$) ($V_R = 25 \text{ Vdc}, T_J = 150^\circ\text{C}$) ($V_R = 70 \text{ Vdc}, T_J = 150^\circ\text{C}$)	I_R	- - -	- - -	2.5 30 50	μAdc
Capacitance (between I/O pins) ($V_R = 0 \text{ V}, f = 1.0 \text{ MHz}$)	C_D	-	0.8	1.5	pF
Capacitance (between I/O pin and ground) ($V_R = 0 \text{ V}, f = 1.0 \text{ MHz}$)	C_D	-	1.6	3	pF
Forward Voltage ($I_F = 1.0 \text{ mAdc}$) ($I_F = 10 \text{ mAdc}$) ($I_F = 50 \text{ mAdc}$) ($I_F = 150 \text{ mAdc}$)	V_F	- - - -	- - - -	715 855 1000 1250	mV _{dc}

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

3. Include SZ-prefix devices where applicable.

Curves Applicable to Each Cathode

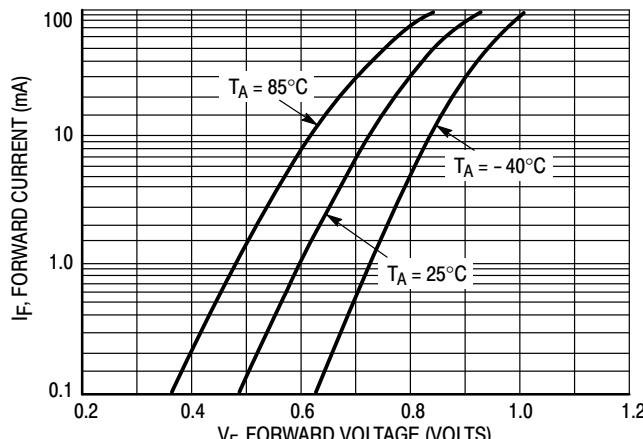


Figure 1. Forward Voltage

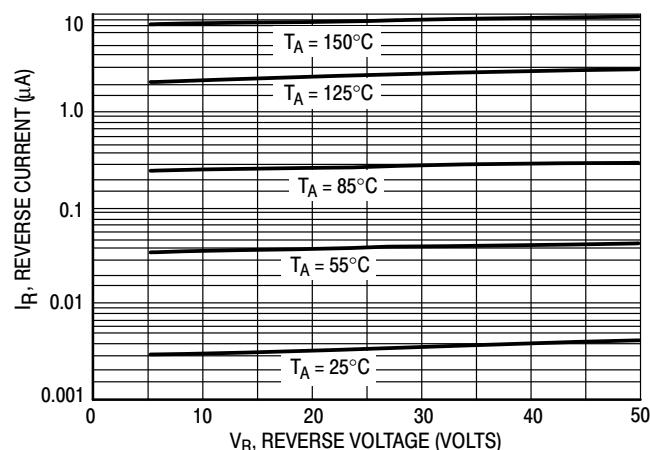


Figure 2. Leakage Current

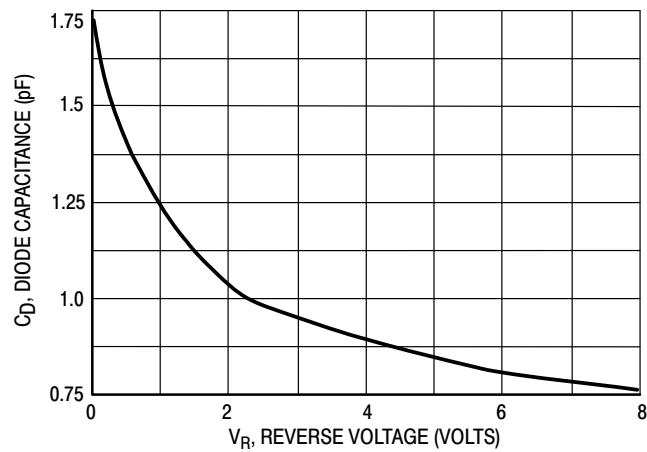


Figure 3. Capacitance